

EE45700 Design/Simulation Assignment
8-bit parallel to serial converter

- This assignment is due on 5/10/22
- Use LTSpice
- Use logisim (<http://www.cburch.com/logisim/>) to verify your logic design before circuit level implementation
- Show your hand analysis for the design (typed)
- Everything must be typed
- Use IEEE journal format (located [here](#))
- Must label figures as well as equations used
- The report consists of: Introduction, design methodology (justification for topologies used), analysis, simulation results and conclusion.
- Use the 0.35um transistors provided in the ee457_035.lib

Design an 8-bit parallel to serial converter with complementary serial outputs as seen in figure 1. The circuit is composed of three stages, the logic, the shift register and the buffer output.

The device works as follows (refer to figure 1):

1. When the parallel-load input $\overline{PL}$ is LOW, parallel data from the inputs D0 to D7 are loaded into the register asynchronously.
2. When $\overline{PL}$ is HIGH, data enters the register serially at the input DS. It shifts one place to the right ($Q0 \rightarrow Q1 \rightarrow Q2$, etc) with each positive-going clock transition.
3. The inputs have schmitt triggers which makes them tolerant for slower input rise and fall times

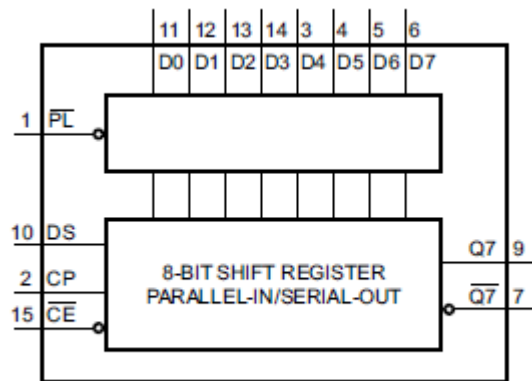


Figure 1: 8-bit parallel to serial converter Functional Block diagram

Table 1: Function Table

Operating modes	Inputs					Qn registers		Output	
	PL	CE	CP	DS	D0 to D7	Q0	Q1 to Q6	Q7	Q7
parallel load	L	X	X	X	L	L	L to L	L	H
	L	X	X	X	H	H	H to H	H	L
serial shift	H	L	↑	l	X	L	q0 to q5	q6	$\overline{q6}$
	H	L	↑	h	X	H	q0 to q5	q6	$\overline{q6}$
	H	↑	L	l	X	L	q0 to q5	q6	$\overline{q6}$
	H	↑	L	h	X	H	q0 to q5	q6	$\overline{q6}$
hold "do nothing"	H	H	X	X	X	q0	q1 to q6	q7	$\overline{q7}$
	H	X	H	X	X	q0	q1 to q6	q7	$\overline{q7}$

- [1] H = HIGH voltage level;
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition;
L = LOW voltage level;
l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition;
q = state of the referenced output one set-up time prior to the LOW-to-HIGH clock transition;
X = don't care;
↑ = LOW-to-HIGH clock transition.

Table 2: Pin Description

Symbol	Pin	Description
$\overline{PL}$	1	parallel enable input (active LOW)
CP	2	clock input (LOW-to-HIGH edge-triggered)
$\overline{Q7}$	7	complementary serial output from the last stage
GND	8	ground (0 V)
Q7	9	serial output from the last stage
DS	10	serial data input
D0 to D7	11, 12, 13, 14, 3, 4, 5, 6	parallel data inputs
$\overline{CE}$	15	clock enable input (active LOW)
V _{cc}	16	positive supply voltage

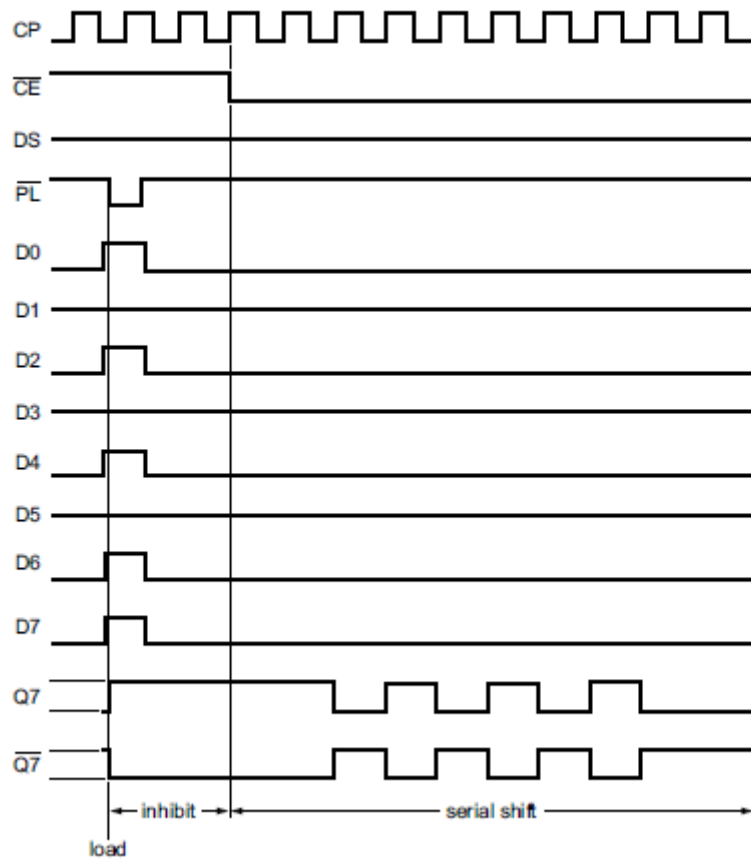


Figure 2. Timing diagram

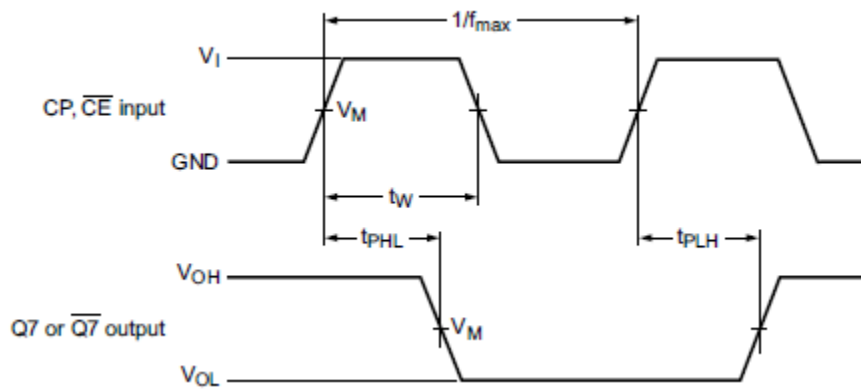


Figure 3. Clock pulse (CP) and clock enable ($\overline{CE}$) to output (Q7 or $\overline{Q7}$) propagation delays, clock pulse width (t_w) and maximum frequency (f_{max})

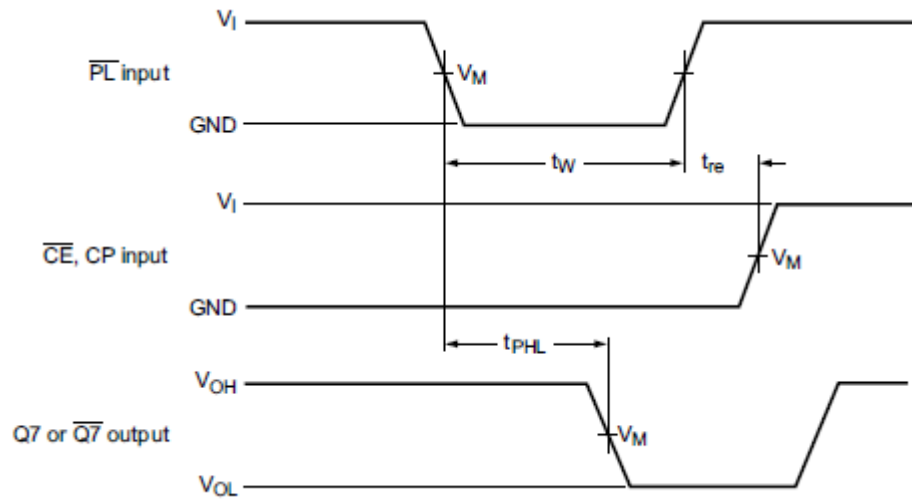


Figure 4. Parallel load ($\overline{PL}$) pulse width, parallel load to output ($Q7$ or $\overline{Q7}$) propagation delays, parallel load to clock (CP) and clock enable ($\overline{CE}$) recovery time

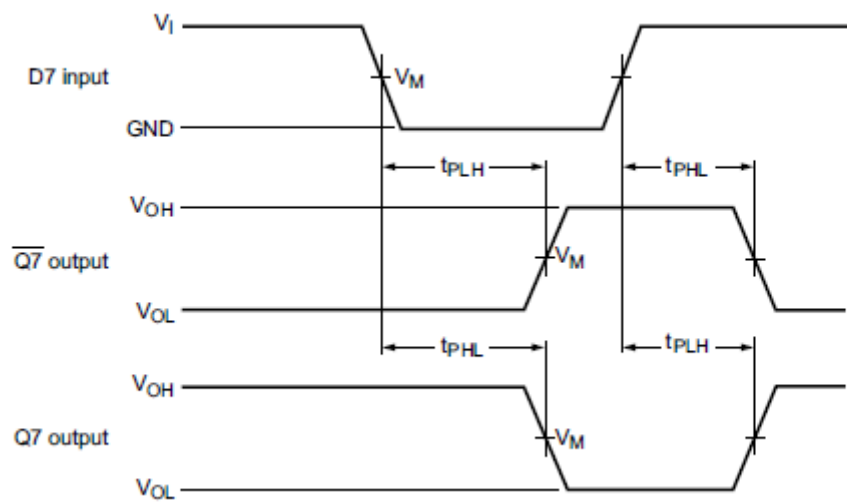


Figure 5. Data input ($D7$) to output ($Q7$ or $\overline{Q7}$) propagation delays when $\overline{PL}$ is LOW.

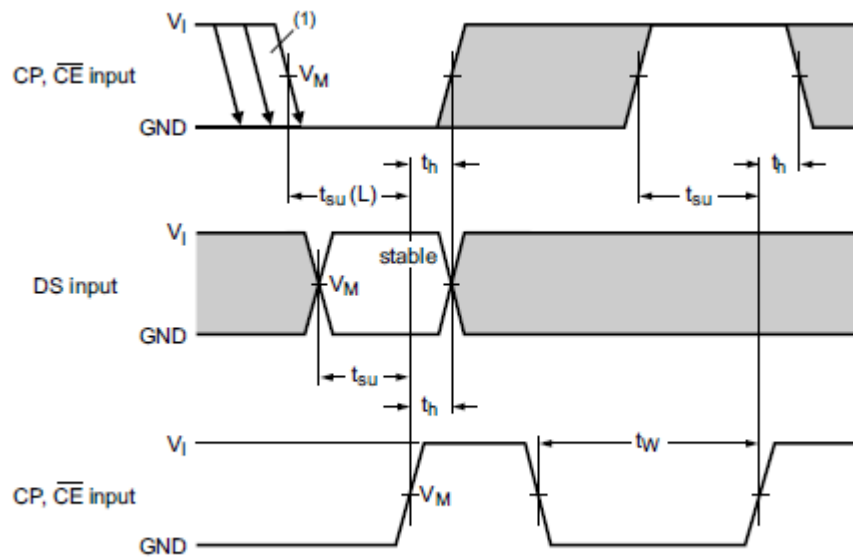


Figure 6. Set-up and hold times. $\overline{CE}$ may change only from HIGH-to-LOW while CP is LOW. The shaded areas indicate when the input is permitted to change for predictable output performance.

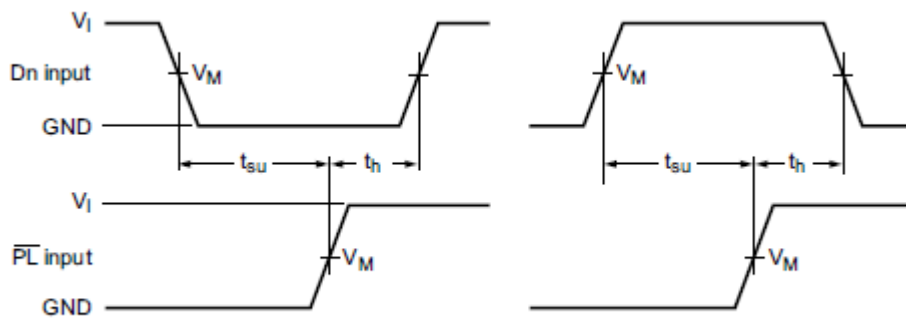


Figure 7. Set-up and hold times from the data inputs (Dn) to the parallel load input ($\overline{PL}$)

Implementation and Constraints

At the on-set of the project, you are to choose one of the following logic families: CMOS, pseudo-NMOS, pass transistor or dynamic. In addition, you must optimize the circuit as to minimize propagation delay

Power Supply: A power supply voltage of 3.3V should be used.

Technology: 0.35um CMOS Process

Load capacitance: Each output bit (Q_7 and $\overline{Q_7}$) shall have a **15 pF load**.

Performance metric: The propagation delay is defined as the time interval between the 50% transition point of the inputs and the 50% point of the worst-case output signal. Note that for dynamic designs, any duty cycle may be used for the clock, but the propagation delay is defined as the distance between the 50% point of the pre-charge clock, until the worst-case output has reached the 50% point (it does incorporate the sum of pre-charge and evaluation periods)!

VOH, VOL, Noise margins: You are free to choose your logic swing. The noise margins should at least be 10% of the voltage swing. Test this by computing the VTC between one of the inputs and the output signals (with the other outputs set to the appropriate values) for a static design. For a dynamic circuit, apply an input signal with a 10% value added to the input and observe the outputs.

Rise and fall times: All input signals and clocks have rise and fall times of 1 nsec.

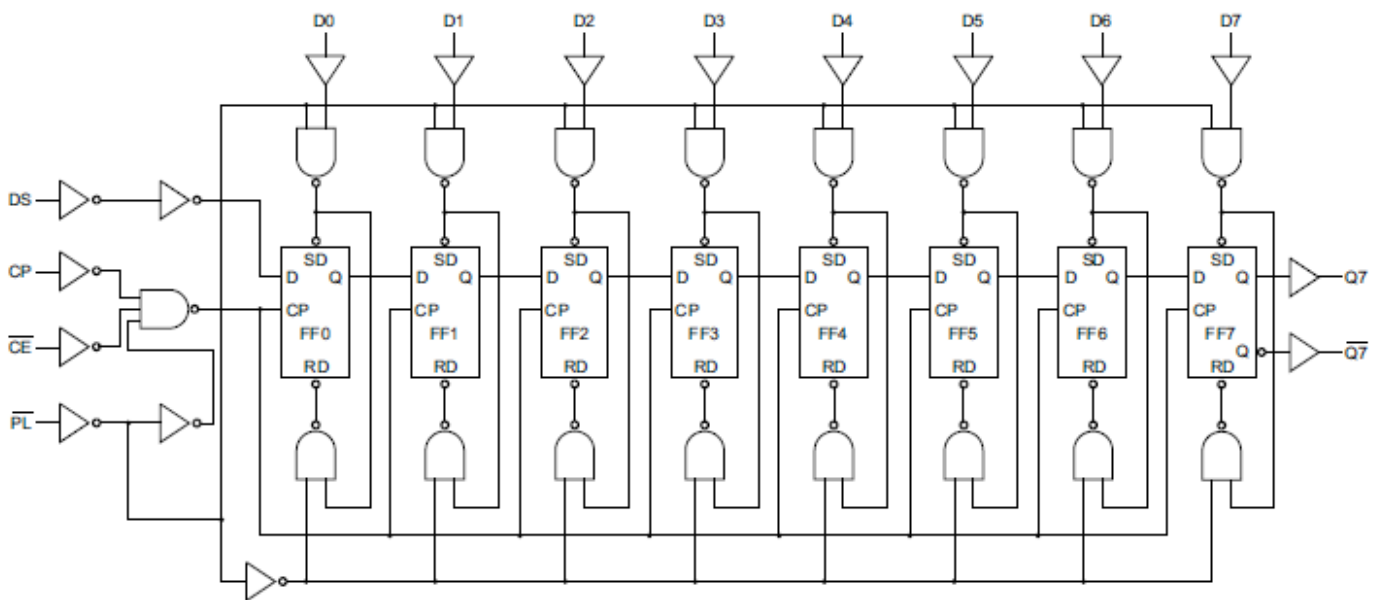


Figure 8. Logic diagram

Your report must a least include:

- Justification for topology used as well as logic family selection
- Logic diagram (flip flops, latches and gates)
- Design of each logic block (including the flip flop and or latch) using the logic family of your choice
- Schematics (with device size information) of the designed gates and flip flops
- Simulations of the full circuit using transient analysis
- Plots of transient waveforms (like figures 2-7) showing functionality (you can choose the period of the waveforms -based on the propagation delays of your circuit- used for the excitation as well as the clock) for both parallel and serial inputs
- Create a table showing DC characteristics: V_{IH} , V_{IL} , V_{OH} , V_{OL} , I_{CC}
- Create a table showing transient characteristics: t_{PHL} , t_{PLH} , t_w , t_{su} , t_h , t_r and t_f (see figures 3-7 for definitions)
- Populate the tables below and include items on (g) and (h)

Static Charateristics				
Symbol	Parameter	Conditions	Value	Units
V_{IH}	HIGH level input voltage	$V_{CC}=3.3V$		V
V_{IL}	LOW Level input voltage	$V_{CC}=3.3V$		V
V_{OH}	HIGH level ouput voltage	$V_{CC}=3.3V$, $I_o=50\mu A$		V
V_{OL}	LOW Level ouput voltage	$V_{CC}=3.3V$, $I_o=50\mu A$		V
I_{CC}	supply current	$V_{CC}=3.3V$, $I_o=0A$		μA
C_i	input capacitance			pF

Dynamic Charateristics				
Symbol	Parameter	Conditions	Value	Units
t_{pd}	propagation delay	CEB, CP to Q7, Q7B, $CL=15pF$		ns
t_w	pulse width	CP input HIGH to LOW		ns
t_{re}	recovery time	PLB to CP, CEB		ns
t_{su}	setup time	DS to CP, CEB		ns
t_h	hold time	DS to CP, CEB; PLB to CP, CEB		ns
f_{max}	maximun frequency	CP input; $CL=15pF$		MHz

Note: $CEB = \overline{CE}$, $PLB = \overline{PL}$, $Q7B = \overline{Q7}$